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10/058,264	01/29/2002	Koji Tomioka	NEC01P260-HYa	4190

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EXAMINER	
NGUYEN, THUONG	
ART UNIT	PAPER NUMBER
2455	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/058,264	TOMIOKA, KOJI	
	Examiner	Art Unit	
	TINA T. NGUYEN	2455	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/26/09*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12,14-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12,14-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on 5/26/09. Claims 9 & 12 were amended. Claims 2-12, 14-20, 22-24 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-12, 14-20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahalingam, Patent No. 6,205,503 in view of Horst, Patent No. 5,867,501.

Mahalingam teaches the invention substantially as claimed including method for the hot swap and add of input/output platforms and devices (see abstract).

4. As to claim 2, Mahalingam teaches a computer system comprising:

a plurality of central processing units (CPU] and memory installed apparatuses having at least one CPU and at least one memory (figure 2) ;

a plurality of input/output control apparatuses (figure 3); and

a network connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other (figure 2),

wherein each of said CPU and memory installed apparatuses comprises communication means for transmitting an input/output instruction issued by at least one

CPU of said plurality of CPU and memory installed apparatuses to at least one of said input/output control apparatuses assigned in advance to said at least one CPU and memory installed apparatuses via said network, and receives a response from at least one of said input/output control apparatuses via said network (figure 2; col 4, lines 28-50; Mahalingam discloses that the system of CPUs, memories and I/O devices communicate with each other via network),

wherein each of said input/output control apparatuses comprises communication means for receiving an input/output instruction from at least one CPU and memory installed apparatuses assigned in advance to at least one of said plurality of input/output control apparatuses via said network, and transmits a response to said input/output instruction to said at least one CPU and memory installed apparatuses via said network (figure 2; col 4, lines 28-50; col 5, lines 65 - col 6, lines 15; Mahalingam discloses that the system of CPUs, memories and I/O devices communicate via network), and

wherein when one of said plurality of diagnostic control circuits detects a fault in a connected CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between a non-faulty CPU and memory installed apparatus and an input/output control apparatus originally connected to a faulty CPU and memory installed apparatus (figure 11A & 12A; col 4, lines 65 – col 5, lines 3; col 5, lines 35-50; Mahalingam discloses that the system of detected a new connection and replaced failed components).

But Mahalingam failed to teach the claim limitation wherein a plurality of diagnostic control circuits, each diagnostic control circuit of said plurality of diagnostic

control circuits being connected with one of said plurality of the CPU and memory installed apparatuses, and with one of said plurality of input/output control apparatuses, and each of said plurality of diagnostic control circuits being connected to one another.

However, Horst teaches the limitation wherein a plurality of diagnostic control circuits, each diagnostic control circuit of said plurality of diagnostic control circuits being connected with one of said plurality of the CPU and memory installed apparatuses, and with one of said plurality of input/output control apparatuses, and each of said plurality of diagnostic control circuits being connected to one another (figure 4 & 5; col 18, lines 35-50; col 82, lines 45-50; col 83, lines 20-50).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Horst so that the system would be able to diagnose the failing CPU and retrieve the connection for the CPU and the memory. One would be motivated to do so to incorporate fault tolerance into data processing.

5. As to claim 3, Mahalingam and Horst teach a computer system as recited in claim 2, wherein means for receiving the input/output instruction as being effective only when the source of the input/output instruction received via said network is a CPU and memory installed apparatuses which has been set in advance (col 7, lines 59-65; Mahalingam discloses that the system of configured the setting in advanced).

6. As to claim 4, Mahalingam and Horst teach a computer system as recited in claim 2, wherein means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatuses which has been set in advance (figure 2; col 8, lines 10-15; Mahalingam discloses that

the system of allows the system to access the elements only when the memory has been configured in advance).

7. As to claim 5, Mahalingam and Horst teach a computer system as recited in claim 2, wherein said network is also used for communications between said plurality of CPU and memory installed apparatus (figure 2).

8. As to claim 7, Mahalingam and Horst teach a computer system as recited in claim 5, wherein means for communicating with other CPU and memory installed apparatuses via said network (figure 3).

9. As to claim 8, Mahalingam and Horst teach a computer system as recited in claim 7, wherein the communications between said plurality of CPU and memory installed apparatuses are communications for accessing memories installed on other CPU and memory installed apparatus (figure 2).

10. As to claim 9, Mahalingam and Horst teach a computer system as recited in claim 2. But Mahalingam failed to teach the claim limitation wherein means for assigning said input/output control apparatuses which have been used by faulty CPU and memory installed apparatuses to another normal CPU and memory installed apparatuses when said faulty CPU and memory installed apparatuses fail to operate, thereby to continue system operation.

However, Horst teaches the limitation wherein means for assigning said input/output control apparatuses which have been used by faulty CPU and memory installed apparatuses to another normal CPU and memory installed apparatuses when said faulty CPU and memory installed apparatuses fail to operate, thereby to continue

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system operation (figure 4 & 5; col 18, lines 35-50; col 82, lines 45-50; col 83, lines 20-50).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Horst so that the system would be able to diagnose the failing CPU and retrieve the connection for the CPU and the memory. One would be motivated to do so to incorporate fault tolerance into data processing.

11. As to claim 10, Mahalingam and Horst teach a computer system as recited in claim 9, wherein an active one of the CPU and memory installed apparatuses which is using another input/output control apparatuses is used as said other normal CPU and memory installed apparatus (figure 5; col 10, lines 3-13; Mahalingam discloses that the system of keeping track of the configured information for all the elements).

12. As to claim 11, Mahalingam and Horst teach a computer system as recited in claim 9, wherein a backup CPU and memory installed apparatus, said backup CPU and memory installed apparatuses being used as said other normal CPU and memory installed apparatus (col 4, lines 33-50; Mahalingam discloses that the system of using the secondary processor in case of the failure in the system).

13. As to claim 14, Mahalingam teaches a CPU and memory installed apparatuses comprising:

at least one central processing unit (CPU) and at least one memory (figure 2);

communication means for communicating with an external circuit comprising an input/output control apparatus, transmitting an input/output instruction issued by said CPU to said input/output control apparatuses which has been assigned in advance, and

receiving a response from said input/output control apparatus (figure 2 & 6; col 4, lines 28-50; Mahalingam discloses that the apparatus of CPUs, memories and I/O devices communicate with each other via network);

wherein when said diagnostic control circuit detects a fault in said connected CPU and memory installed apparatus, said diagnostic control circuit retrieves previously stored information that determines a new connection between a second non-faulty CPU and memory installed apparatus and an input/output control apparatus originally connected to a faulty CPU and memory installed apparatus (figure 11A & 12A; col 4, lines 65 – col 5, lines 3; col 5, lines 35-50; Mahalingam discloses that the apparatus of detected a new connection and replaced failed components).

But Mahalingam failed to teach the claim limitation wherein a diagnostic control circuit connected with said CPU and said at least one memory and with said input/output control apparatus; a single board on which said CPU, said memory, said diagnostic control circuit and said communication means are mounted.

However, Horst teaches the limitation wherein a diagnostic control circuit connected with said CPU and said at least one memory and with said input/output control apparatus (figure 1; col 2, lines 57-68); a single board on which said CPU, said memory, said diagnostic control circuit and said communication means are mounted (figure 1; col 2, lines 57-68).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Horst so that the system would be able to diagnosed CPU group, main memory access controller and IOP group. One would be

motivated to do so to detect the presence of an abnormal element by diagnose the multiprocessor system, including CPU elements.

14. As to claim 18, Mahalingam and Horst teach a computer system as recited in claim 2, wherein each of said plurality of input/output control apparatuses further comprises an input/output (I/O) device (figure 2).

15. As to claim 19, Mahalingam and Horst teach a computer system as recited in claim 18, wherein said input/output (I/O) device is connected to a peripheral device (col 4, lines 65 – col 5, lines 3; Mahalingam discloses that the system of connecting the devices to a peripheral device).

16. As to claim 20, Mahalingam and Horst teach a computer system as recited in claim 18, wherein said input/output (I/O) device is connected to a second network (figure 6).

17. As to claim 22, Mahalingam and Horst teach a computer system as recited in claim 2, wherein said communication means comprises a plurality of ports (figure 1).

18. As to claim 23, Mahalingam and Horst teach a computer system as recited in claim 22, wherein each of said plurality of input/output control apparatuses is allocated to at least one of said plurality of ports of said communication means (figure 5).

19. As to claim 24, Mahalingam and Horst teach a computer system as recited in claim 22. But Mahalingam failed to teach the claim limitation wherein when one of the plurality of CPU and memory installed apparatuses stops its operation with one of said plurality of input/output control apparatuses, said one of said plurality of input/output

control apparatuses is newly allocated to any one of the plurality of ports to which said one of said plurality of input/output control apparatuses was not previously allocated.

However, Horst teaches the limitation wherein when one of the plurality of CPU and memory installed apparatuses stops its operation with one of said plurality of input/output control apparatuses, said one of said plurality of input/output control apparatuses is newly allocated to any one of the plurality of ports to which said one of said plurality of input/output control apparatuses was not previously allocated (col 4, lines 48 – col 5, lines 28).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mahalingam in view of Horst so that the system would be able to determine the fault elements and disconnected that element from the groups. One would be motivated to do so to diagnosed elements from the CPU and non-CPU groups.

20. Claims 6, 15 disclose a computer system, a CPU and memory claims and do not teach or define any new limitations above claim 4 and therefore are rejected for similar reasons.

21. Claim 12 disclose a computer system claim and do not teach or define any new limitations above claim 9 and therefore are rejected for similar reasons.

22. Claim 16 disclose an input/output claim and do not teach or define any new limitations above claim 14 and therefore are rejected for similar reasons.

23. Claim 17 disclose an input/output control claim and do not teach or define any new limitations above claim 3 and therefore are rejected for similar reasons.

Response to Arguments

Applicant's arguments with respect to claims 2-12, 14-20, 22-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TINA T. NGUYEN whose telephone number is (571)272-3864, and the fax number is 571-273-3864. The examiner can normally be reached on 9:00AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Saleh Najjar can be reached on 571-272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Examiner, Art Unit 2455

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